Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A1**
2. **OUT 1**
3. **IN 1**
4. **V –**
5. **GND**
6. **IN 4**
7. **OUT 4**
8. **A4**
9. **A3**
10. **OUT 3**
11. **IN 3**
12. **NC**
13. **V +**
14. **IN 2**
15. **OUT 2**
16. **A2**

**.093”**

**.113”**

**10 9 8 7**

**15 16 1 2**

**11**

**13**

**14**

**DIE ID**

**HI201HS**

**6**

**5**

**4**

**3**

**MASK**

**REF**

**C50013A1**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V- (or leave Floating)**

**Mask Ref: 50013A1**

**APPROVED BY: DK DIE SIZE .096” X .113” DATE: 8/25/21**

**MFG: HARRIS/INTERSIL THICKNESS .020” P/N: HIO-201-2**

**DG 10.1.2**

#### Rev B, 7/19/02